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Description

STRUCTURES AND METHODS FOR MAKING STRAINED MOSFETS

BACKGROUND OF INVENTION

[0001] The invention generally relates to making MOSFETs with vertical gates of strained Si, and more particularly relates to making single gate and double gate MOSFETS and fin-FETS with vertical gates of strained Si.

[0002] As semiconductor devices shrink, traditional device fabrication techniques have approached practical limits in size scaling. For example, as channel lengths shrink below about 50 nm, devices start to exhibit short channel effects including threshold voltage rolling off for shortened channel lengths. Unwanted short channel effects may be reduced by higher doping concentrations, which lead to the unwanted effects of carrier mobility degradation, increased parasitic junction capacitance, and increased subthreshold swing if doping concentrations become too high.

[0003] One method to minimize short channel and reverse short channel effects includes striking an optimum doping profile by well controlled implantation and annealing. However, carefully controlling implantation and annealing adds costs to the fabrication process, and are ultimately limited in effectiveness as channel lengths are further reduced. Scaling limits imposed due to the limitation of gate oxide thickness and source/drain junction depth may also arise to impair function of the smaller devices.

[0004] Another method to achieve further reduced scale includes difficult to manufacture profiles for the channel. Such profiles include double gate, triple gate, quadruple gate, omega-gate, pi-gate, and finFET MOSFET designs. Some of these designs are plagued with design problems such as gate alignment errors leading to increased parasitic capacitance.

[0005] Another possible way to avoid some scaling problems is to improve device performance by improving material performance. For example, strained Si produces higher mobility of carriers resulting in faster and/or lower power consumption devices. Due to changes in strained Si crystalline structure (i.e. its symmetry and lattice constant are different due to its strain state), a strained Si film has

electronic properties that are superior to those of bulk Si. Specifically, the strained Si could have greater electron and hole mobilities, which translate into greater drive current capabilities for n-type and p-type transistors, respectively. Accordingly, devices incorporating strained Si may have improved performance without necessarily reducing device size. However, where the strained Si does allow for further scaling, performance improvement will be further improved.

[0006] It should be noted, however, an important criteria in enabling high-performance devices by utilizing strained Si is the fabrication of a low-defect-density strained Si film. In particular, reducing the number of dislocations in the strained Si film is especially important in order to reduce leakage and improve carrier mobility.

[0007] Growing a Si layer on a substrate having lattice parameters different from the Si, generates the strained Si film. Accordingly, the number of defects in the strained Si film may be proportional to the number of defects in the underlying substrate on which the film is grown. An increase in the number of dislocations in the Si channel can increase the leakage current in the device while in the "off" stage. When formed improperly, the strained Si film can

contain a high number of defects and the subsequent strained Si film will then exhibit poor performance characteristics, and any benefits of using a strained Si film will be substantially negated.

[0008] Accordingly, producing strained Si films having minimal defects such as dislocations is desirable for further reduction in semiconductor device size and power requirements. Thin strained Si films having few defects may lead to improved semiconductor device performance

SUMMARY OF INVENTION

[0009] In one aspect of the invention, a method comprises forming a relaxed SiGe block on a substrate and forming a strained Si film on the substrate adjacent at least one side of the relaxed SiGe block. The method further includes forming a gate oxide on a side of the strained Si film to form a strained channel region.

[0010] In another aspect, the invention includes a method comprising forming a relaxed SiGe block on an oxide substrate and forming a first nitride spacer on a top of the relaxed SiGe block. A second nitride spacer is formed on the oxide substrate adjacent a first side of the relaxed SiGe block and a side of the first nitride spacer, and a strained Si film is epitaxially formed on a second side of

the relaxed SiGe block.

[0011] In still another aspect, the invention includes a channel for a semiconductor device comprising a fin of strained Si vertically oriented on a non-conductive substrate.

Brief Description of Drawings

[0012] Figures 1-8 illustrate steps in forming an embodiment in accordance with the invention; Figures 9-14 illustrate steps in forming devices in accordance with the invention; and Figures 15-19 illustrate further steps in forming an embodiment in accordance with the invention.

Detailed Description

[0013] The invention relates to forming MOSFETs with channels of strained Si. In the invention, transistor performance is enhanced by creating thin films of strained Si. Due to the small dimension of the strained Si, when it is formed, such as by epitaxial growth techniques, the defect density (i.e. dislocation) is typically very low. Such a low defect film may be produced by forming a vertical SiGe bar or block on a relaxed SiGe-on-oxide wafer. One side of the SiGe bar or block may be covered with nitride. The other side of the vertical SiGe bar or block may be covered with a small dimensioned Si film using a selective eptiaxial

growth process. The Si film will be strained due to mismatch of the lattice constants with the SiGe substrate. Due to the small dimensions of the Si film and the relaxed structure of the SiGe substrate, the tendency for dislocation formation is reduced. After completion, the strained Si can be subjected to further processing to build various types of MOSFETS such as finFETs with single, double, or more gates.

[0014] Figure 1 illustrates a relaxed SiGe layer 12 on an oxide wafer 10. Although an oxide wafer is used in this example, any non-conductive substrate suitable for semiconductor device fabrication may be used. The relaxed SiGe layer 12 may be formed on the oxide wafer 10 by any of the suitable methods known in the art such as wafer binding or oxygen implantation annealing. In one embodiment, the SiGe layer 12 may range between 30 nm and 80 nm in thickness, although other thicknesses are contemplated by the invention.

[0015] Figure 2 shows a thin oxide layer 14 deposited over the relaxed SiGe layer 12. A first polysilicon layer 16 is formed on the oxide layer 14. Next, a photoresist 18 is deposited on the first polysilicon layer 16 and patterned so a portion of the first polysilicon layer 16 is covered by the photore-

sist 18 and a portion of the first polysilicon layer 16 is exposed. Typical thicknesses for the thin oxide layer 14 range from about 5 nm to 20 nm, and 40 nm to 100 nm for the first polysilicon layer 16. Each layer is formed by methods which are well known in the art.

[0016] Figure 3 illustrates the results of an etching process where the exposed portion of the first polysilicon layer 16 and underlying thin oxide layer 14 are etched away leaving a portion of the first polysilicon 16. The etching process uses known methods to selectively etch polysilicon and oxide. The photoresist layer 18 has also been removed after etching the first polysilicon 16 and oxide layer 14. Accordingly, a first portion of the SiGe layer 12 lies exposed and a second portion of the SiGe layer 12 is covered with the thin oxide layer 14 and first polysilicon layer 16. Next, a first nitride spacer 20 is formed on top of the SiGe layer 12 abutting the edge of the thin oxide layer 14 and first polysilicon layer 16 using any of the nitride forming processes well known in the art.

[0017] Figure 4 shows a further etching step in which the exposed SiGe layer 12 is selectively etched using an etching process similar to those described with reference to Figure 3. In Figure 4, the portion of the relaxed SiGe layer 12

not covered by the first nitride spacer 20, and the thin oxide layer 14 and first polysilicon layer 16, is etched away to expose a portion of the underlying oxide wafer 10. A second nitride spacer 22 is then formed on the exposed portion of the oxide wafer 10, abutting the edges of the etched relaxed SiGe layer 12. The first nitride spacer 20 lies adjacent to a second larger nitride spacer 22.

[0018] Figure 5 illustrates the results of selectively etching the remaining portions of the first polysilicon layer 16 and thin oxide layer 14. The portion of the relaxed SiGe layer 12 underlying the thin oxide layer 14 and first polysilicon layer 16 is etched away in this process. Consequently, the relaxed SiGe shaped as a SiGe block 24 remains from the original relaxed SiGe layer 12 on top of the oxide wafer 10. The SiGe block 24 is surrounded on one side by the second nitride layer 22 and on the top by the first nitride spacer 20, leaving one side of the SiGe block 24 exposed.

[0019] Figure 6 illustrates a "strained"Si film 26 epitaxially grown on the exposed side of the SiGe block 24. A selective growing process is used so that the Si film 26 is formed only on the exposed portion of the SiGe block 24. In this process, the Si film 26 has a height greater than its thickness and is vertically oriented on the surface of the oxide

wafer 10. Because the Si film 26 may be formed with substantially any aspect ratio (height divided by thickness) including those greater than 1, the Si film 26 may be characterized as a "fin"vertically oriented on the oxide wafer 10.

[0020] Additionally, the Si film 26 may be approximately the same height as the SiGe block 24. Accordingly, the height of the Si film 26 may be controlled by adjusting the height of the layer of the relaxed SiGe layer 12. The height of the SiGe layer 12 may be controlled during its formation by methods well known in the art. Furthermore, the thickness of the Si film 26 may be controlled during the growing process by suitable methods well know in the art of device fabrication. The Si film 26 may range from about 50 Å(Angstroms) to about 200 Å in thickness, although other thicknesses may be used where needed.

[0021] The Si film 26 may be used as the channel in a semiconductor device in virtually any type of device benefiting from a channel having a reduced number of defects and/or having small dimensions. Accordingly, at least one gate oxide may be formed on a portion of the Si channel with source/drain regions formed in the Si film 26 on either side of the gate oxide. The resulting structure, because it

is vertically oriented, allows access to both sides and a top of the channel from above the substrate. This geometry allows the gate oxide to surround the channel, and allow for almost total depletion of the channel to be achieved in the off state. It also allows both sides of the source/drain regions to be accessed for better doping and better lead connectivity.

[0022] By growing the Si film 26 on a surface of the relaxed SiGe block 24, the number of defects such as dislocations in the resulting Si film 26 are reduced. Dislocations in the Si film 26 are also minimized because only a thin film of small size is grown. Additionally, the strained Si film acquires its internal strain due to its crystal lattice being formed on the SiGe crystal lattice. That is, the SiGe block 24 has a crystal lattice constant (different dimensions between the atoms) than that of the Si film, i.e. , standing alone, Si would normally have a smaller lattice constant than the SiGe because the lattice constant of the Si material does not match the lattice constant of the SiGe. However, in the structure of the invention, the lattice structure of the Si layer will tend to match the lattice structure of the SiGe. By virtue of the lattice matching of the Si (which normally is smaller) to the SiGe mask, the Si layer is

placed under a tensile stress. That is,the SiGe mask will try to obtain an equilibrium state thus resulting in a stress of an Si sidewall layer formed on the SiGe. This volume of stressed Si may act as a strained channel. Accordingly, the Si film 26 may be described as a low defect strained Si fin or channel.

[0023] Figure 7 shows the formation of a gate oxide 28 using ion implantation on the exposed side of the Si film 26. V_t (threshold voltage) ion implantation techniques may be used, for example, and the implantation angle may be tilted towards gate oxide 28 on the side. Examples of gate oxide 28 thicknesses range from about 9 Åto about 20 Å, although other thicknesses may be formed when required. It is also possible to use high "k"materials, such as HfO_2, to replace the oxide as a gate dielectric.

[0024] Figure 8 shows a second polysilicon layer 30 deposited over the first and second nitride spacers, 20 and 22, SiGe block 24, Si film 26 and gate oxide 28. Although the second polysilicon layer 30 is shown as a conformal layer, a non-conformal layer, or a layer with a topography somewhere between conformal and non-conformal may be formed as required for subsequent steps of device formation. As an example, the polysilicon layer 30 may range

from a thickness of about 700 Åto about 1500 Å.

[0025] From the configuration illustrated in Figure 8, various devices may be fabricated including, for example, strained Si MOSFETs such as, for example, a finFET with a single strained gate or a finFET with a strained double gate. Figures 9-14 show an example of fabricating a single-gate device, and Figures 15-19 show an example of fabricating a double-gate finFET type device. Additionally, a tri-gate device, with the gte dielectric wrapping around the top and two sides of the strained Si film may also be fabricated from the structure shown in Figure 8. Although examples of a single-gate device and double-gate finFET type device are shown, any type of device which may benefit from a vertical strained Si film with reduced dislocations may be fabricated from the illustrated structure shown in Figure 8.

[0026] Referring to Figure 9, a top view of the device being fabricated is illustrated with a photoresist 102 deposited and patterned over the second polysilicon layer 30. As shown in Figure 9, the photoresist 102 is deposited over the second polysilicon layer 30 in the region of the Si film 26 which will form the gate of the resulting device. Figure 10 illustrates a side view of the structure of Figure 9 with the

photoresist 102 over the second polysilicon layer 30.

[0027] Figure 11 illustrates a top view of the resulting structure after etching the photoresist 102 of Figure 9 using etching processes known in the art such as wet etching. In particular, the etching step leaves what will become two source/drain regions 104, one on either side of a gate region 106. In the source/drain regions 104, the oxide wafer 10, gate oxide 28 on the side and top of the underlying Si film 26, and second nitride spacer 22 are exposed. The Si film 26 is not visible in Figure 11.

[0028] Figure 12 illustrates a cross section of the device shown in Figure 11. As illustrated in Figure 12, an ion implantation is performed in the source/drain regions 104 to form extensions on either side of the gate region 106. Any ion implantation process appropriate for source/drain implantation for the device being fabricated may be used as is well known in the art. Large tilt angle ion implantation, with energy levels of, for example, of about 0.2 1 keV for boron implantation or 1 2 keV for arsenic, may additionally be used.

[0029] Figure 13 illustrates a top view of the device being fabricated after nitride spacers 108 are formed by nitride deposition onto the oxide wafer 10 adjacent the second

polysilicon layer 30, and subsequent etching. Figure 14 illustrates the nitride spacers 108 overlaying the gate oxide 28 and second nitride spacer 22. After forming the nitride spacers 108, further processing steps including source/drain implantation and annealing may be carried out, as appropriate for the device being fabricated.

[0030] Starting with the structure shown in Figure 8, Figure 15 illustrates a subsequent step in the formation of a strained Si double gate finFET, which is an example of another type of device in which the strained Si film included in the invention may be implemented. As shown in Figure 15, an oxide film 202 is deposited, and planarized using, for example, CMP (chemical mechanical planarizing). The remaining oxide film 202 is then etched leaving a portion of the second polysilicon layer 30 exposed above the oxide film 202. The oxide film 202 may be deposited using, for example, directional HDP (high density plasma) to preferentially deposit most of the oxide on the flat surfaces and less oxide on the top of the polysilicon 30 in the region above the nitride spacers, 20 and 22.

[0031] Figure 16 illustrates etching a portion of the second polysilicon layer 30 to leave a portion of the first and second nitride layers, 20 and 22, exposed. Suitable etching

processes may include any process to selectively etch polysilicon and any etching process, such as a wet etch, to selectively etch the oxide. After etching, the first and second nitride spacers, 20 and 22, are exposed and protrude above the second polysilicon layer 30. The second polysilicon layer 30 will form a raised region in the vicinity of the bases of the first and second nitride spacers, 20 and 22, and gate oxide 28.

[0032] Figure 17 illustrates the results of wet selective etching of the two nitride spacers, 20 and 22 a wet etching of the SiGe block 24. Throughout the fabrication process, typical etchants which may be used to etch nitride include, for example, fluorine and chlorine. Selective etching of Si_3N_4 to SiO_2 may be performed with a boiling H_3PO_4 solution (e.g., 85% H_3PO_4 at 180° C) because this solution attacks SiO_2 very slowly. The etch rate is ~10nm/min for Si_3N_4, but less than 1 nm/min for SiO_2. Si_3N_4 is etchable at room temperature in concentrated HF or buffered HF. However, HF also etches SiO_2. Using a reactive ion plasma etching process, the following etch chemistries may be used for Si_3N_4: CHF_3/O_2; CH_2F_2; CH_2CHF_2. By removing the SiGe block 24 and the first and second nitride spacers, 20 and 22, the strained Si 26 film has a side exposed for further

processing, such as, for example, adding another gate oxide.

[0033] Figure 18 illustrates forming a second gate oxide 208 by a gate oxidation process which forms a thin oxide layer 204 and 205 over the exposed portions of the device and Si film 26, respectively. In particular, the portion of the thin oxide layer 205 formed over the Si film 26 constitutes a second gate oxide 208 portion of the gate oxide 205. The gate oxide 205 also includes the first gate oxide 207 formed in an earlier step. The second gate oxide 208 may be formed by, for example, a thermal oxide growing process to produce a high quality oxide.

[0034] Also shown in Figure 18 is a thin polysilicon layer deposited over the surface of the device. The structure is then subjected to a direct etch to form thin polysilicon spacers 206 on the sides of the thin oxide layer 204. In particular, a thin polysilicon spacer 206 is formed adjacent the second gate oxide 208. The polysilicon spacers 206 may protect the gate oxide 208 from further etching processes. The thin polysilicon spacers 206 may be, for example, about 100 Å thick. Additionally, the thin polysilicon spacers 206 are formed to leave portions of the thin oxide layer 204 exposed on the top portions of the sec-

ond polysilicon layer 30.

[0035] Figure 19 illustrates etching the exposed portions of the thin oxide layer 204. Any process which selectively etches an oxide layer may be used to remove the exposed portions of the thin oxide layer 204. After the oxide etching is completed, polysilicon is deposited to form a third polysilicon layer 210 over the substrate. The resulting structure includes a fin of strained Si 26 standing vertical to the oxide wafer 10 surrounded on its sides and top by a gate oxide 205. Both of the sides of the vertical fin of strained Si 26 are accessible from above the surface of the oxide wafer 10. Furthermore, the vertical fin of strained Si 26 also includes source/drain regions with both of their sides and top accessible from above the oxide wafer 10.

[0036] It is possible to continue processing the device illustrated in Figure 19 to produce a completed double-gate finFET device having a strained Si film with fabrication steps well known in the art.

[0037] While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims. For example, the invention can be readily applicable to bulk substrates.